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| EXAMINER | |
|---|---|
| PEREZ, JAMES M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2611 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/533,058 | SANDULEANU, MIHAI ADRIAN TIBERIU | |
| | Examiner | Art Unit | |
| | James M. Perez | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/27/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## *Detailed Action*

### *Drawings*

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because Figure 2 does not explicitly show how the clock inputs to elements 21-24 are connected. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet

submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moser (USPN 6853696) in view of Savoj (Design of Half-Rate Clock and Data Recovery Circuits for Optical Communication Systems).

With regards to claim 1, Moser teaches a Phase Locked Loop (PLL) (col. 1, lines 25-30, and 40-45) comprising

a frequency detector including an unbalanced quadricorrelator, (fig. 2: col. 7, lines 7-16), comprising

a frequency detector including clocked bi-stable circuits (fig. 2: elements 26a,b: col. 7, lines 30-35) coupled to a first multiplexer and to a second multiplexer (fig. 2:

elements 28 and 32) being controlled by a signal having a same bitrate as the incoming signal (fig. 2: elements 28, 32, and DATA: col. 6, lines 12-17), and

a phase detector (fig. 2: elements 38, and 34a,b: col. 7, line 36 through col. 8, line 25) controlled by a first signal provided by the first multiplexer and by a second signal provided by the second multiplexer (elements 38, and 34a,b: col. 7, line 36 through col. 8, line 25).

Moser does not explicitly teach the use of double edge clocked bi-stable circuits and the signals output from first and second multiplexers being a pair of signals.

Savoj teaches a frequency detector which uses double edge clocked bi-stable circuits (fig. 11: section 3.2.2: two double-edge-triggered flipflops); and

the signals output from first and second multiplexers being a pair of signals (figs. 11 and 12: section 3.2.2-3.2.3: V1, V2, Vpd1 and Vpd2).

Therefore it would be obvious to one of ordinary skill in the art at time of the invention to combine quadricorrelator frequency detection circuit of Moser with double-edge flipflop and frequency detection circuit of Savoj in order to provide an improved performance in frequency detector in order to better utilize a wider range of frequencies while reducing the required size of the circuitry (Savoj: Abstract and Introduction).

With regards to claim 2, Moser in view of Savoj teach the limitations of claim 1.

Moser further teaches the frequency detector comprises a first pair of clocked bi-stable (fig. 2: elements 30a,b: col. 7, lines 36-49) circuits coupled to the first multiplexer (fig. 2: element 32), and a second pair of clocked bi-stable circuits (fig. 2: elements

26a,b: col. 7, lines 30-35) coupled to the second multiplexer (fig. 2: element 28), which first and second pairs are supplied by mutually quadrature phase shifted signals (fig. 2: col. 6, lines 12-49 and col. 7, lines 8-49) respectively to provide the first signal and the second signal (fig. 2: FQ1 and FQ2).

Moser does not explicitly teach the use of double edge clocked bi-stable circuits and the signals output from first and second multiplexers being a pair of signals, wherein the first pair and the second pair indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals.

Savoj teaches a frequency detector which uses double edge clocked bi-stable circuits (fig. 11: section 3.2.2: two double-edge-triggered flipflops);

the signals output from first and second multiplexers being a pair of signals (figs. 11 and 12: section 3.2.2-3.2.3: V1, V2, Vpd1 and Vpd2), wherein

the first pair and the second pair indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals (figs. 11 and 12: section 3.2.2-3.2.3: V1, V2, Vpd1 and Vpd2).

Therefore it would be obvious to one of ordinary skill in the art at time of the invention to combine quadricorrelator frequency detection circuit of Moser with double-edge flipflop and frequency detection circuit of Savoj in order to provide an improved performance in frequency detector in order to better utilize a wider range of frequencies while reducing the required size of the circuitry (Savoj: Abstract and Introduction).

With regards to claim 5, Moser in view of Savoj teaches the limitations of claim 2.

Moser further teaches a Phase Locked Loop, wherein

the mutually quadrature phase shifted signals are generated by a voltage controlled oscillator (fig. 4: elements VCO, ICK and QCK).

With regards to claim 6, Moser in view of Savoj teaches the limitations of claim 5.

Moser further teaches the error signal is inputted to a coarse control input of the voltage controlled oscillator (fig. 1: elements 8, 14, 6 and 2: col. 2, lines 25-30: coarse frequency lock) via a first charge pump (fig. 1: element Charge Pump) coupled to a first low-pass filter (wherein a low-pass filter is a type of loop-filter) coupled to an multiplexer (fig. 1: wherein the phase and frequency error signals are added onto the line input to element 6)

5. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moser (USPN 6853696) in view of Savoj (Design of Half-Rate Clock and Data Recovery Circuits for Optical Communication Systems), further in view of Morgan (USPN 6,320,406).

With regards to claim 3, Moser in view of Savoj teach the limitations of claim 2.

Moser further teaches a Phase Locked Loop, wherein

the phase detector (fig. 2: elements 38, and 34a,b: col. 7, line 36 through col. 8, line 25) comprises

a D flip-flop (fig. 2: elements 38, and 34a,b: col. 7, line 36 through col. 8, line 25) receiving the first signal (fig. 2: elements 34a,b and FQ2: col. 7, line 36 through col. 8, line 25) and being clocked by the second signal (fig. 2: elements 34a,b and FQ1: col. 7, line 36 through col. 8, line 25), the second signal being inputted to respective logic gates, such as NOT and NOR gates (fig. 2: elements 34a,b, FQ3A, 36a,b and NOT gate).

Moser does not teach all but two Limitations: Limitation 1) and the signals output from first and second multiplexers being a pair of signals; and Limitation 2) the second signal being inputted to respective gates of a first transistors pair for determining a state ON or OFF of a current through said first transistors pair.

Limitation 1)

Savoj the signals output from first and second multiplexers being a pair of signals (figs. 11 and 12: section 3.2.2-3.2.3: V1, V2, Vpd1 and Vpd2), wherein

Therefore it would be obvious to one of ordinary skill in the art at time of the invention to combine quadricorrelator frequency detection circuit of Moser with double-edge flipflop and frequency detection circuit of Savoj in order to provide an improved performance in frequency detector in order to better utilize a wider range of frequencies while reducing the required size of the circuitry (Savoj: Abstract and Introduction).

Limitation 2)

Morgan teaches that NOT gates and NOR gates are made up of transistors (fig. 11: elements 110, 1100-1101, 114, 1140-1145: col. 7, line 27 through col. 8, line 21), wherein

the NOT gate (fig. 11: elements 1100-1101) is made of a transistor pair (fig. 11: elements 1100-11: col. 7, lines 35-40); and

the input of the NOT gate is attached to the gates of the first transistor pair for determining a state ON or OFF of a current through said first transistors pair (fig. 11: elements 1100-1101: col. 7, line 27 through col. 8, line 21).

One of ordinary skill in the art would clearly recognize that using transistors to construct logic gates such as NOT and NOR gates is well known and expected in the art as taught by Morgan. Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to use the NOT and NOR gates as disclosed in Morgan in the quadricorrelator of Moser in order to implement a digital quadricorrelator with more accurate determination of frequency error in the quadric and in-phase input signal.

With regards to claim 4, Moser in view of Savoj further in view of Morgan teach the limitations of claim 3.

Moser further teaches the NOT biasing the input (outputting a signal) of the NOR logic gates (fig. 2: elements NOT gate and 36a,b); and

said NOR logic gates generating an output signal indicative for a frequency error between the incoming data signal and Clock signals (fig. 2: OUT+ and OUT-: col. 7, lines 18-28).

Moser does not explicitly teach the current through the first transistor pair biases a second transistor pair, the second transistor pair receiving the first signal pair and generating an output signal.

Morgan teaches the current through the first transistor pair biases a second transistor pair, the second transistor pair receiving the first signal pair and generating an output signal.

Morgan teaches that NOT gates and NOR gates are made up of transistors (fig. 11: elements 110, 1100-1101, 114, 1140-1145: col. 7, line 27 through col. 8, line 21), wherein

the NOT gate (fig. 11: elements 1100-1101) is made of a transistor pair (fig. 11: elements 1100-11: col. 7, lines 35-40); and

the NOR gate (fig. 11: elements 114, 1140-1145) has transistor pairs (col. 7, lines 52-65: transistor pair 1140/1143 and transistor pair 1141/1142: teach pair attached to a particular input of the NOR gate).

One of ordinary skill in the art would clearly recognize that using transistors to construct logic gates such as NOT and NOR gates is well known and expected in the art as taught by Morgan. Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to use the NOT gate and NOR gates as disclosed in Morgan in the quadricorrelator and logic gates disclosed by Moser in order to implement a digital quadricorrelator with more accurate determination of frequency error in the quadric and in-phase input signal.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moser (USPN 6853696) in view of Savoj (Design of Half-Rate Clock and Data Recovery

Circuits for Optical Communication Systems) as applied to claim 6 above, and further in view of Lee (USPN 5,734,301).

With regards to claim 7, Moser in view of Savoj teaches the limitations of claim 6.

Moser further teaches a fine control input is controlled by a signal provided by a phase detector (fig. 1: elements 4, 14, 6, and 2: col. 2, lines 25-40: phase lock condition: note that phase lock is more precise (fine) than a frequency lock (coarse)).

Moser does explicitly teach a phase detector coupled to a second charge pump coupled to second low-pass filter.

Lee teaches a phase detector (fig. 1: element 12) coupled to a second charge pump coupled (fig. 1: element 22) to second low-pass filter (element 22: wherein a low-pass filter is a type of loop filter).

Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to combine the quadricorrelator of Moser with the Dual PLL of Lee in order to create an improved synchronizer unit for synchronizing with data signals encoded in the Non-return to zero (NRZI) inverted scheme.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Perez whose telephone number is 571-270-3231. The examiner can normally be reached on Monday through Friday: 9am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JP
1/22/2008

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SUPERVISORY PATENT EXAMINER